UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/260,794	03/01/1999	DOUGLAS S. ONDRICEK	03401.P090	6932

27520 7590 03/17/2004

FORMFACTOR, INC.
LEGAL DEPARTMENT
2140 RESEARCH DRIVE
LIVERMORE, CA 94550

EXAMINER	
BREWSTER, WILLIAM M	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/260,794	ONDRICEK ET AL.	
	Examiner	Art Unit	
	William M. Brewster	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,7-12,14-26,31-33 and 68-72* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,7-12,14-26,31-33 and 68-72* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 7, 11, 12, 16, 29, 31-33, 68, 69, 70, 72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al., U.S. Patent No. 5,635,832, in view of Wood et al., U.S. Patent No. 5,949,242 in view of Friedman, U.S. Patent No. 6,078,845.

Ito teaches a method comprising: in fig. 10 depositing a die 40 into a carrier 30, in fig. 8, mounting said carrier onto a substrate by placing standoffs 36, col. 5, lines 41-62, on said carrier into sloped positioning holes, in fig. 10, on said substrate 50; with a plurality of freestanding contact elements, wherein said carrier is mounted on said substrate after depositing said dice onto said carrier, on the substrate, testing said singulated dice while deposited in said carrier, col. 6, lines 25-55; in fig. 8, wherein said step of mounting said carrier onto a substrate by standoffs 36 on said carrier into sloped positioning holes 51 and 52 on said substrate 50 causes first contact elements on said plurality of singulated dice inherently causes the wiping second contact elements on said substrate by the pressure asserted; in fig. 11, further comprising applying a top 60 on said carrier after depositing said dice into said carrier, col. 7, lines 23 - col. 8, line 2.

Ito does not specify using resilient electrical contacts, but Wood does. Wood teaches a method comprising: singulating at least one semiconductor wafer into a plurality of singulated dice; in figs. 1, 2, and 3, depositing said plurality of said singulated dice 14 unpackaged into said carrier circuit 32, depositing singulated die into said carrier, said carrier holding said singulated die with or without packaging of die, in fig. 2, storing on a plurality of contact pads 16, and testing said singulated dice while deposited in said carrier, in fig. 4, possibly using elongated resilient electrical contact elements, where a top mounting testing unit would apply more force during testing than after it was removed, col. 4, lines 52-60; in fig. 9 mounting carrier on substrate 10E, at the timing convenience of the manufacturer, which may be a test printed circuit board and which may serve as the final package for said dice, col. 8, lines 5 - 20, with a top 42, containing a hole or opening 60 where a plurality of elongated contacts could pass, and through which a tool, including a labeling tool, may enter, over the die and at any given time, removing die and reusing test board, col. 4, line 5 - col. 5, line 8. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Wood's process with Ito's invention would have been beneficial because resilient clips allow for more flexibility and greater tolerance of misalignment.

Ito and Wood do not specify storing the test results, but Friedman does. Friedman teaches in fig. 3, a method comprising: depositing a plurality or singulated dice into a carrier 18, said carrier comprising a digital storage device 16; and storing in said digital storage device data indicating results of said testing of each of said dice,

further comprising storing an identification code in said digital storage device, wherein said identification code comprises information identifying at least one semiconductor wafer from with dice were singulated, programming digitally where the where lot information includes a panoply of chip information including test results used to determine if the chip passed or failed the test, unique identification to the code, and wafer from which said dice were singulated and the position on the wafer from where the dice came, at least one origin semiconductor wafer information, using data stored in said digital storage device a map of a semiconductor wafer from which at least two of said dice were singulated indicating a location on said wafer of each of said dice and an indication of whether each said die passed or failed said testing, col. 5, lines 4 - 53. Friedman gives motivation in col. 2, line 58 - col. 3, line 3. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Friedman's process with Ito's and Wood's invention would have been beneficial because using the statistical pass/fail information would decrease the time necessary to bring a new device, or process, up to volume manufacturing standards while increasing process yield.

Claims 8-10, 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito, Wood, and Friedman as applied to claims 1, 3, 7, 11, 12, 16, 29, 31-33, 68, 69, 70, 72 above, and further in view of Miyauchi et al., U.S. Patent No. 5,528,825, from IDS.

Ito, Wood, and Friedman do not teach labeling each IC with an identification code, but Miyauchi does. Miyauchi teaches in fig. 3, attaching a bar-code label 11 to an

IC 10, a plurality of elongated contacts (extending down from the chip), col. 2, lines 53 - 56, at any convenient time, and further specifies that 10 may be an unpackaged chip, col. 3, lines 6 - 20. Miyauchi gives motivation in col. 1, lines 53-59. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Ito's, Wood's, and Friedman's process with Miyauchi's invention would have been beneficial because one can select an IC to correct for specific variation.

Response to Arguments

Applicant's arguments with respect to all claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

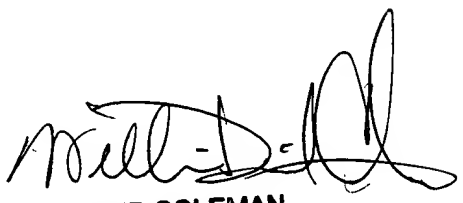
extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 571-272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

8 March 2004
WB



W. DAVID COLEMAN
PRIMARY EXAMINER